Analysis of Better-Than-Worst-Case System Design Methodology by Using Canary Flip-Flops

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We demonstrate a dependable system design methodology using canary FF. Design margins due to process and environmental variations are getting larger and larger as process technology scales down in deep sub-micron domain. Large design margins inevitably decrease system performance and lose the benefits provided by technology scaling. Canary circuits have been proposed to predict system error before it causes catastrophic failures in a similar way that sending canary in mine to detect toxic gas. We use canary flip-flops to predict timing error before it causes system failure. By using canary flip-flops, it enables to design system under typical timing condition rather than worst case limits. When timing error is predicted by canary flip-flop, the error state of circuit is remedied by increasing supply voltage level or decreasing clock frequency. Since replacing all D flip-flops will have severe negative impact on performance, candidate flip-flops should be carefully selected. In order to satisfy this requirement, we have developed a tool that replaces only flip-flops on timing vulnerable paths. Using the tool, we design two conventional 32 bit RISC processors to analyze the area and power overhead by canary flip-flops. In order to decrease area and power overhead, normal D flip-flops are selectively replaced with canary flip-flops. The detail of selective flip-flops replacement algorithm is described in Fig.1. The tool that selectively replaces D flip-flops on critical pathes with canary flip-flops of gate level netlist generated from Synopsys Design Compiler can be provided by request.

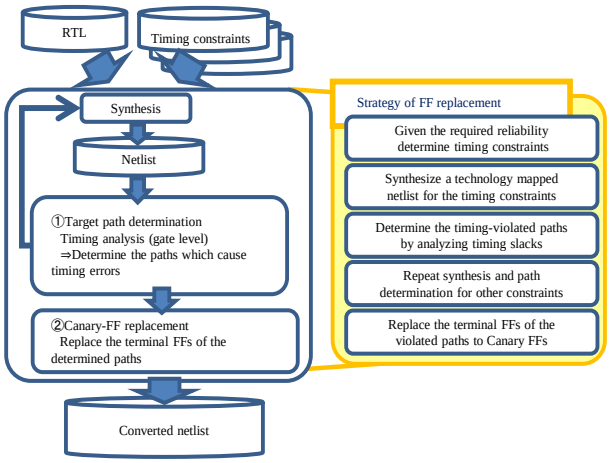

Figure.1 Selective D flip-flops replacement with canary flip-flops

References

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