5.5 GFLOPS Vector Units for "Emotion Synthesis"

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Overview

- Strategy of VU architecture
- VU features and instruction sets
- Examples
- Performance

Strategy of VU Architecture

- Targets
  - Optimized for 3D calculations
  - Easy to develop software pipelined programs
  - Simple hardware
- Solutions
  - VLIW processor
  - 4 parallel fMACs
  - All operations have same pipeline depth
    (Except DIV/SQRT/RSQRT operations)

And one more essence …..

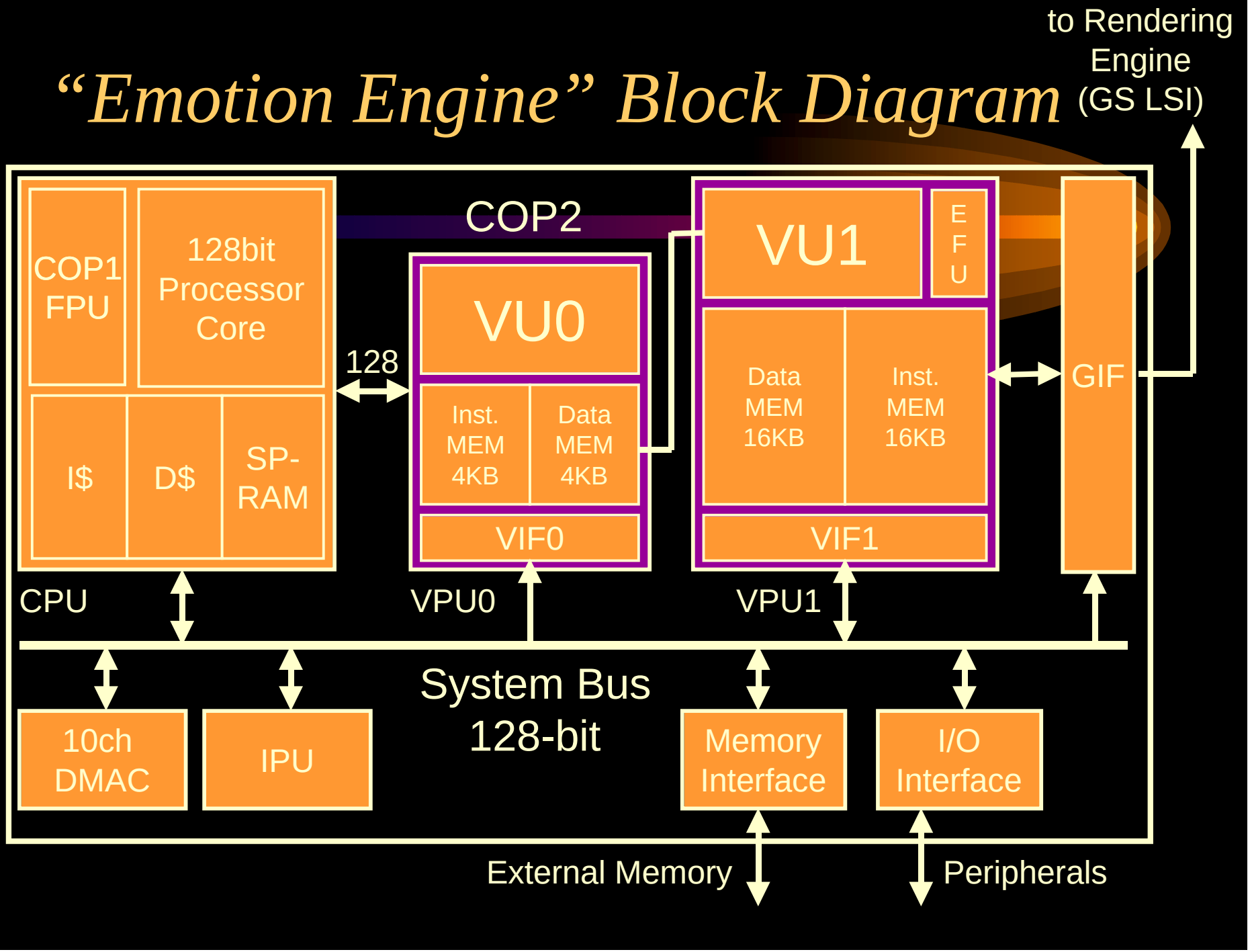
"Emotion Synthesis"

- "Emotion Synthesis"
  - more realistic, more detailed and more natural motions

Need Huge Calculation Power

- We prepared two different of Vector Unit(VU)s
  - VU0 : for flexible calculation with CPU control
  - VU1 : for well-defined 3D calculations

"Emotion Engine" Block Diagram

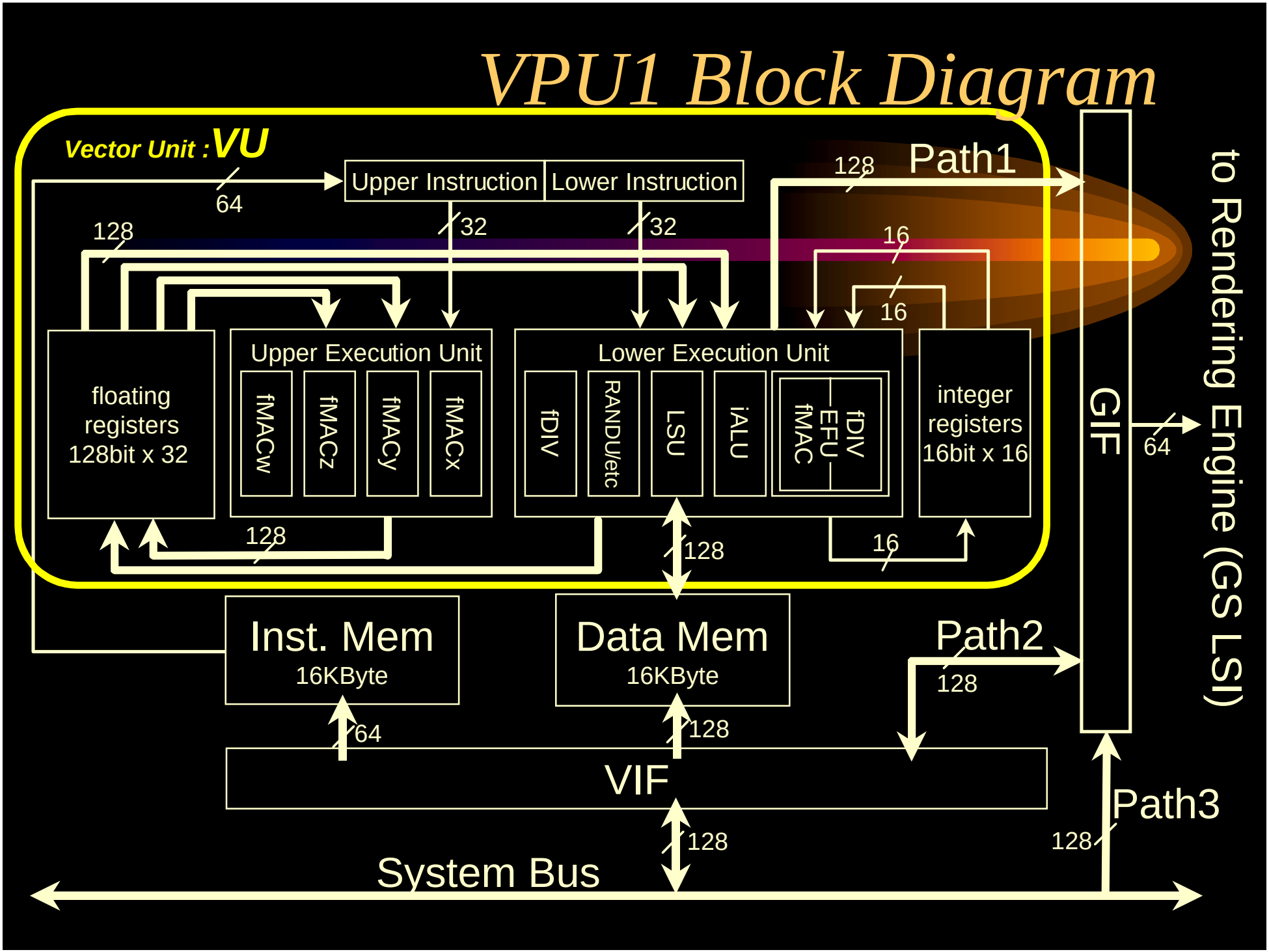


VU

- VLIW mode
  - 64-bit VLIW instruction formats
  - 5 function units are available simultaneously
    - 4 FMAC + (FDIV, Branch, load/store, or iALU)
- Co-processor mode
  - MIPS COP2 instruction : 32-bit opcode
  - Two kinds of COP2 instructions :
    - 4 parallel Floating operations
    - call micro-subroutine of VLIW mode

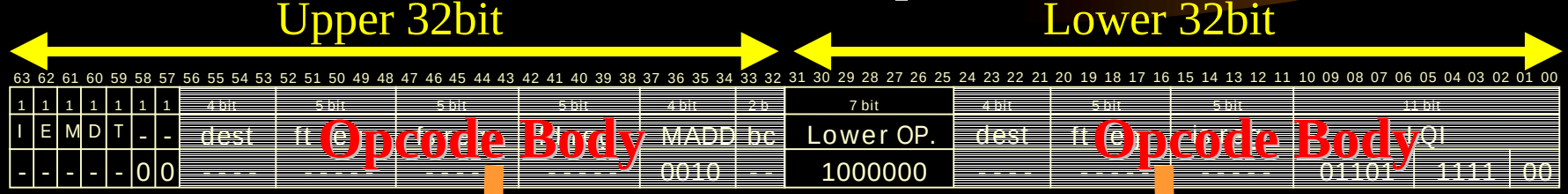
VU0 and VU1

	VU0	**VU1**
Main purpose	Flexible Calculation with CPU control	Well-defined 3D calculations
VLIW mode	Available	Available
Co-processor mode	Available	**N/A**
VPU	With … Inst. memory : **4KB** Data memory : **4KB** VIF(system bus I/F)	With … Inst. Memory : **16KB** Data Memory : **16KB** VIF(system bus I/F) **GIF(Graphics I/F)** **EFU(VU option)**


VPU1 Block Diagram
Vector Unit : VU
64
Upper Instruction
Lower Instruction
32
32
128
Path1
128
16
16
floating registers 128bit x 32
Upper Execution Unit
fMACw
fMACz
fMACy
fMACx
Lower Execution Unit
fDIV
RANDU/etc
LSU
iALU
fDIV EFU fMAC
integer registers 16bit x 16
GIF
64
to Rendering Engine (GS LSI)
128
128
16
Inst. Mem 16KByte
Data Mem 16KByte
Path2
128
64
128
VIF
128
Path3
128
System Bus

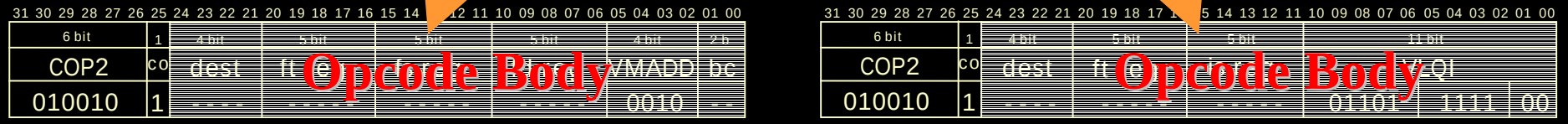
Instruction opcode to support 2 modes

VLIW mode : 64-bit VLIW instruction opcode

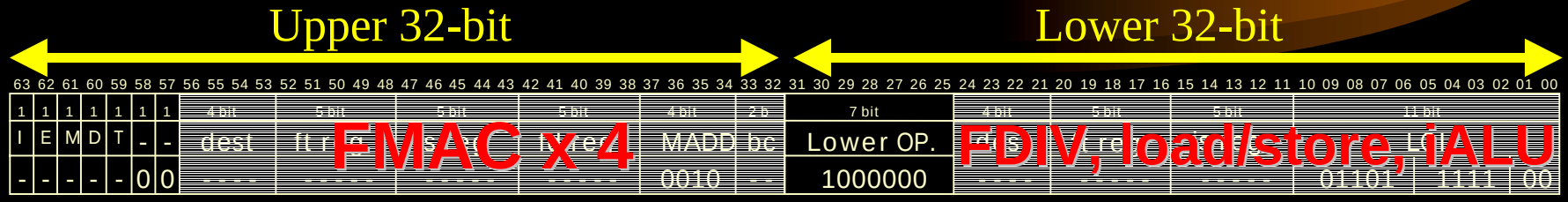


A VLIW instruction includes two COP2 instructions.

Co-processor mode : 32-bit MIPS COP2 instruction opcode



64-bit VLIW instruction



Upper Instructions :

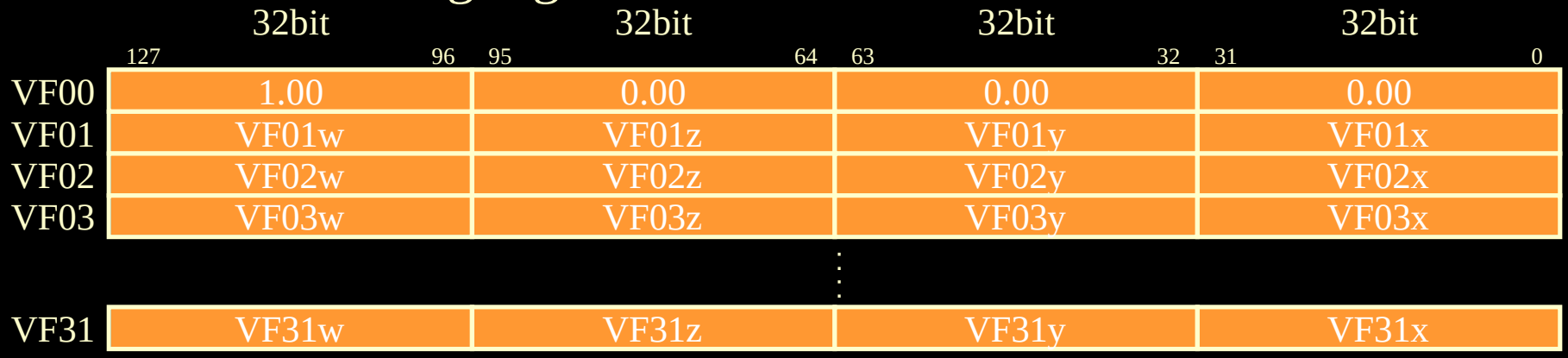
- 4 parallel floating ADD/SUB
- 4 parallel floating MUL
- 4 parallel floating MADD/MSUB
- 4 parallel floating MAX/MIN
- Outer product calculation
- Clipping detection

Lower Instructions :

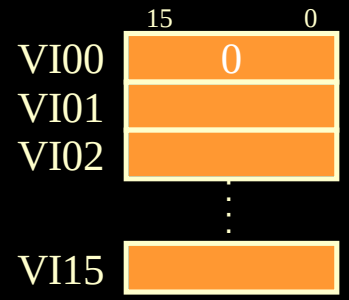
- Floating DIV/SQRT/RSQRT
- Load/Store 128-bit data(4 FP data)
- Jump/Branch
- Elementary Function Unit
- Random Unit

Registers

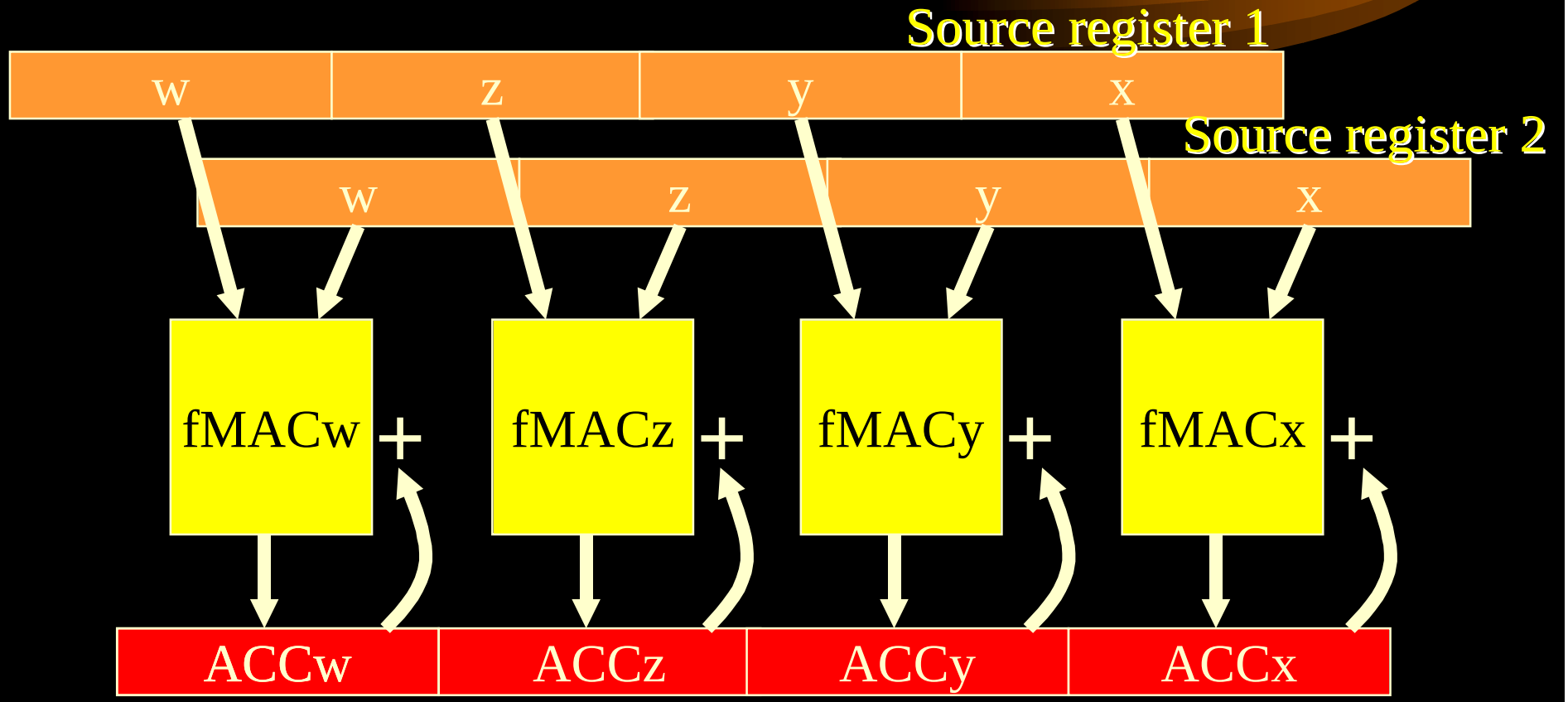
128-bit floating register x 32



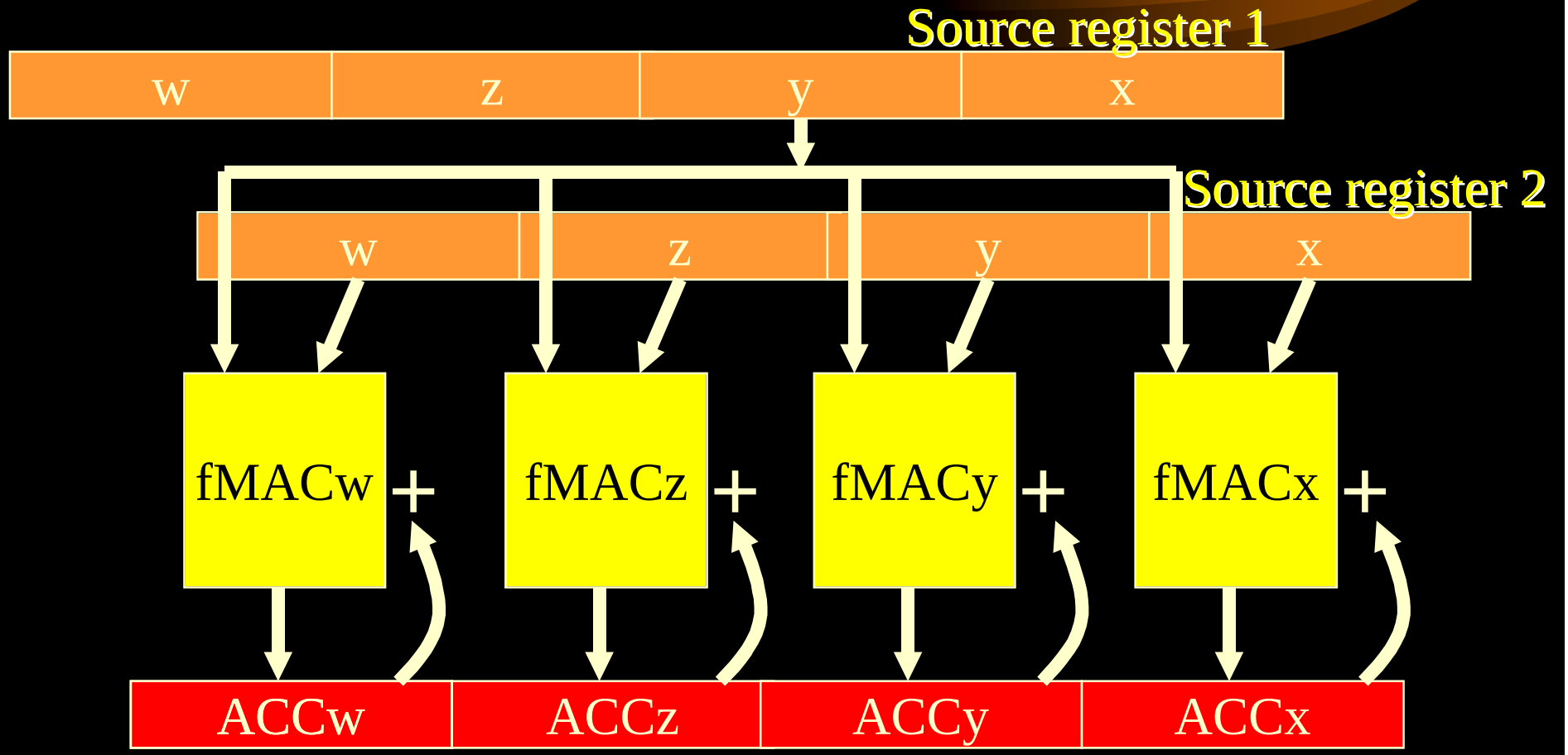
16-bit integer register x 16



4 Parallel FMADD



4 Parallel FMADD with Broadcast



VLIW mode Pipeline Stages

- 3 cycle Latency : Basic Operations

ADD, SUB, MUL, MADD, MSUB
load/store, iALU operations, e.t.c.

- 7 cycle Latency : DIV / SQRT

DIV

SQRT

- 13 cycle Latency : RSQRT

RSQRT

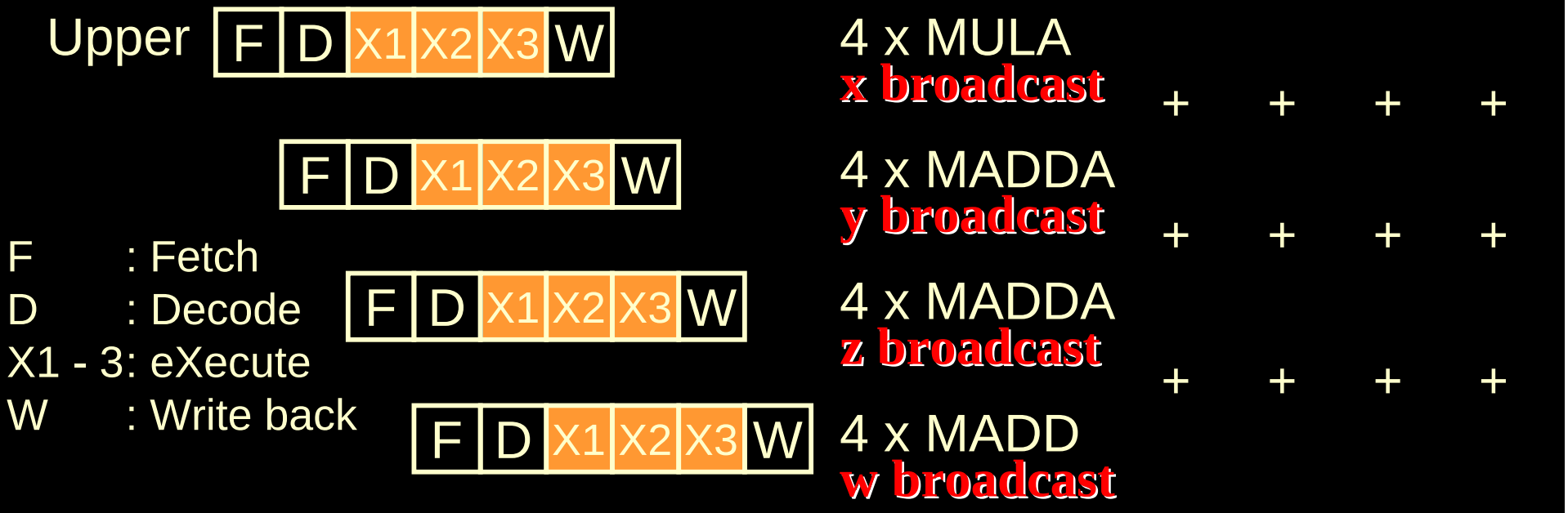
Geometry Transformation

$$
\begin{aligned}
FMACx: & \\
FMACy: & \\
FMACz: & \\
FMACw: &
\end{aligned}
\begin{pmatrix}
m_{00} & m_{01} & m_{02} & m_{03} \\
m_{10} & m_{11} & m_{12} & m_{13} \\
m_{20} & m_{21} & m_{22} & m_{23} \\
m_{30} & m_{31} & m_{32} & m_{33}
\end{pmatrix}
\begin{pmatrix} x \\ y \\ z \\ w \end{pmatrix}
$$

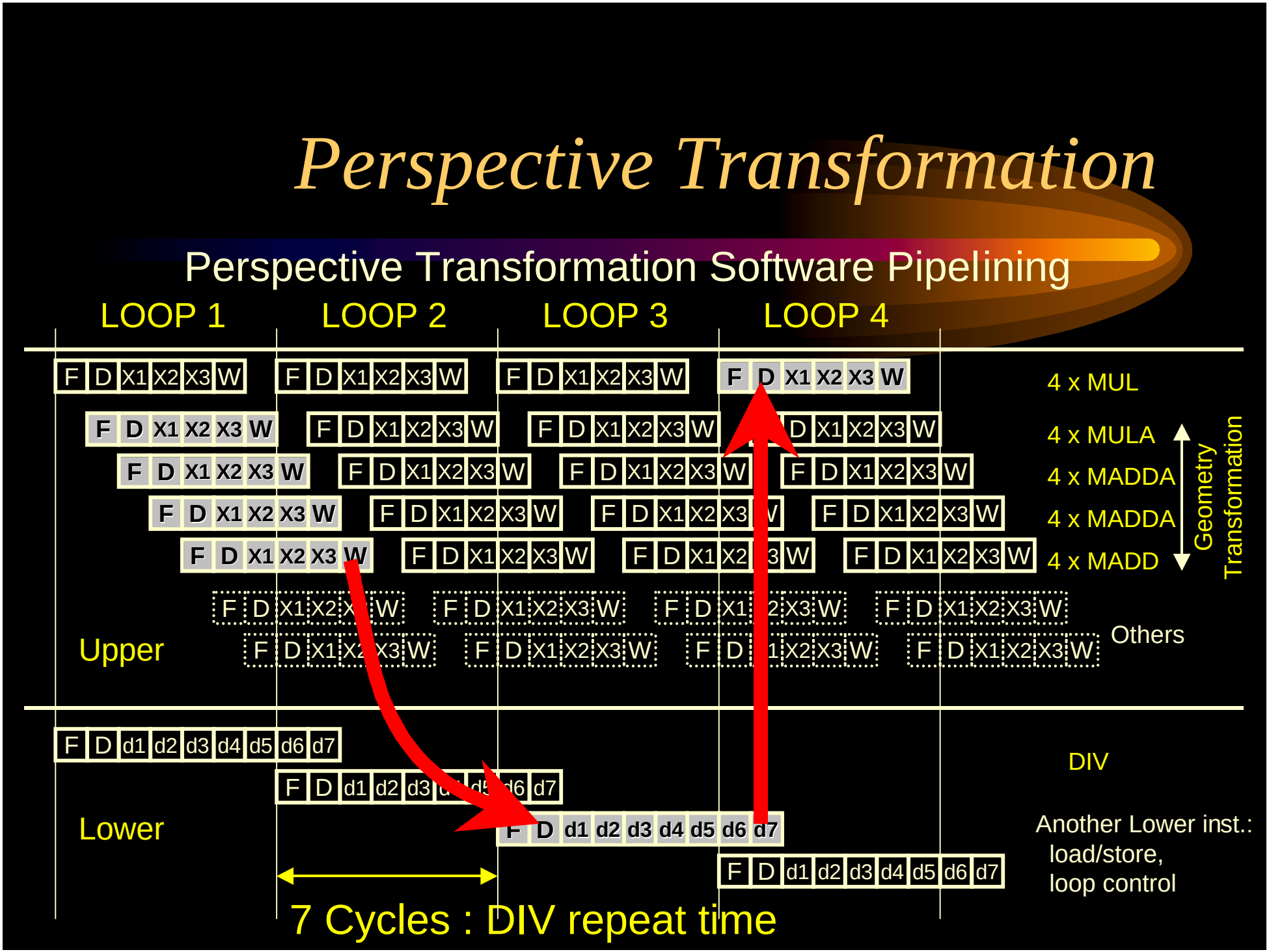
$$
= \begin{pmatrix}
m_{00}x + m_{01}y + m_{02}z + m_{03}w \\
m_{10}x + m_{11}y + m_{12}z + m_{13}w \\
m_{20}x + m_{21}y + m_{22}z + m_{23}w \\
m_{30}x + m_{31}y + m_{32}z + m_{33}w
\end{pmatrix}
$$

Geometry Transformation Pipeline

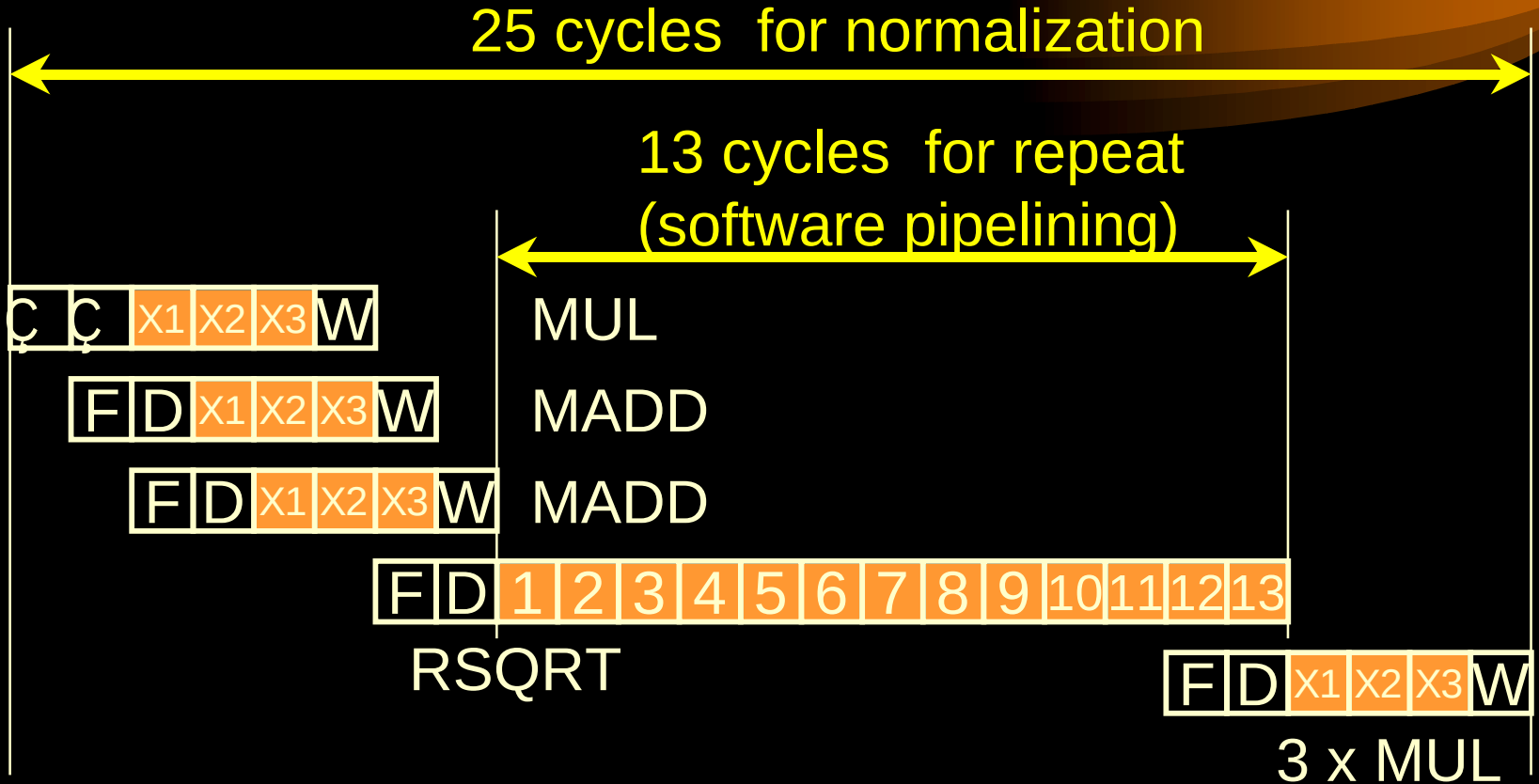
Geometry Transformation Pipeline



Perspective Transformation

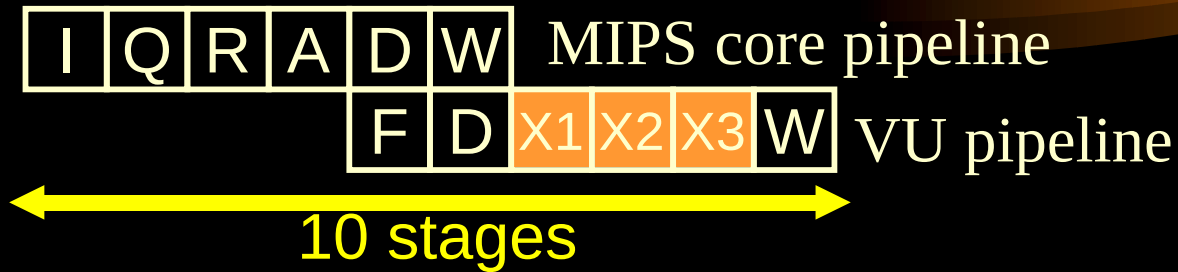


Vector Normalization

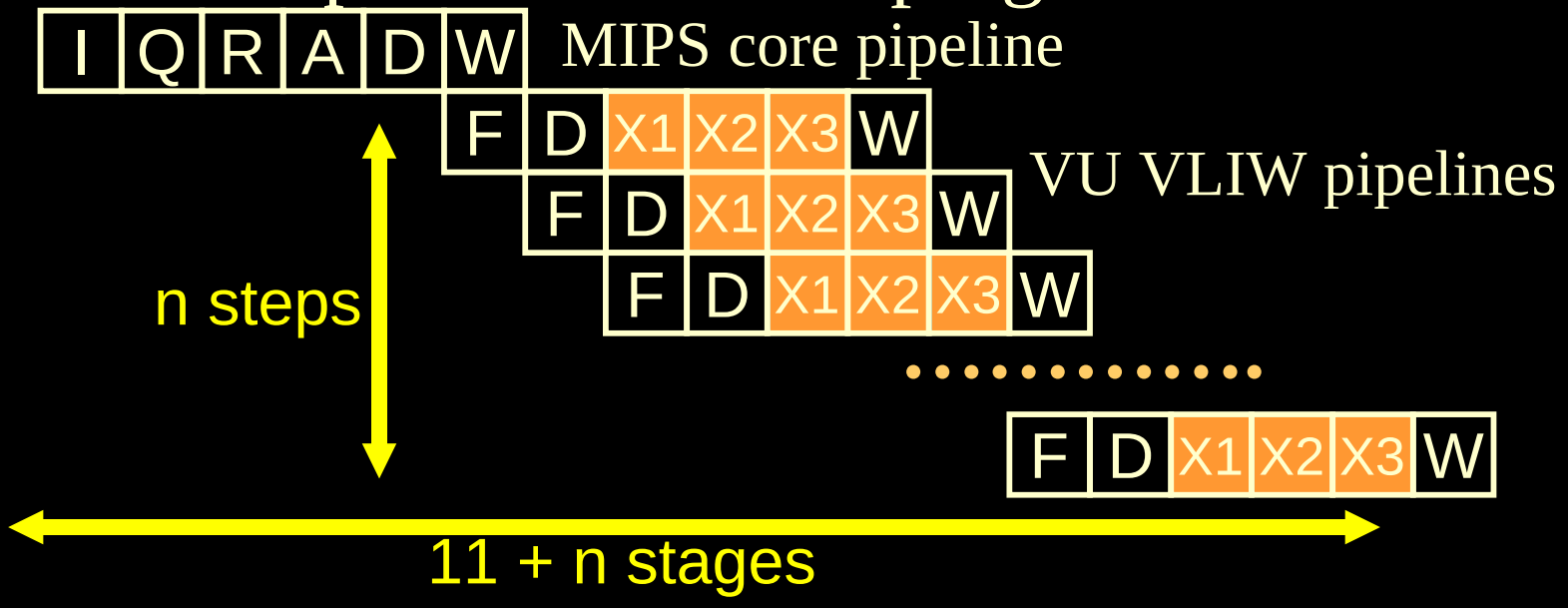


Co-processor Mode Pipeline stages

- Basic operations

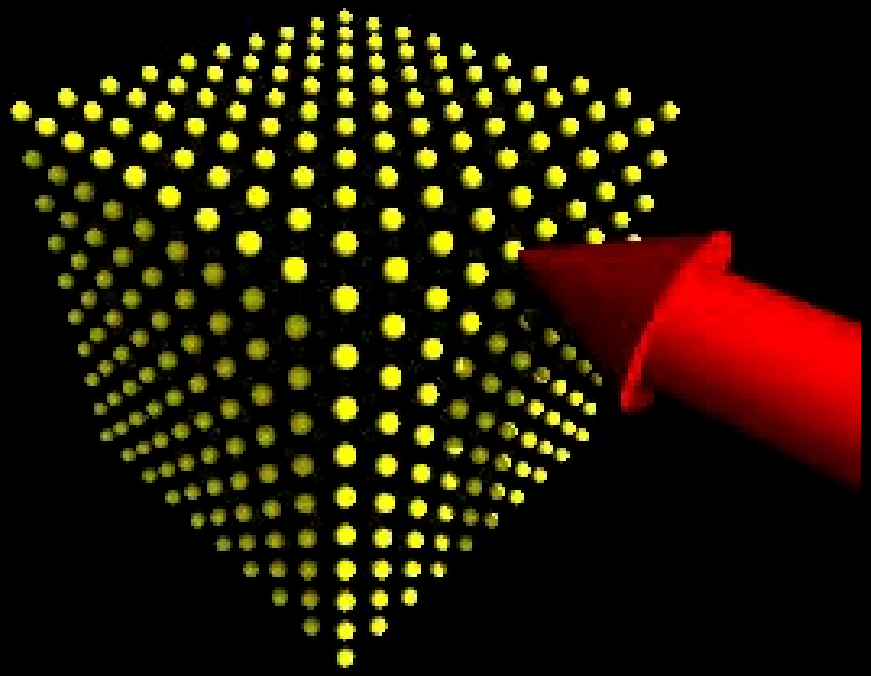


- call VLIW processor mode programs



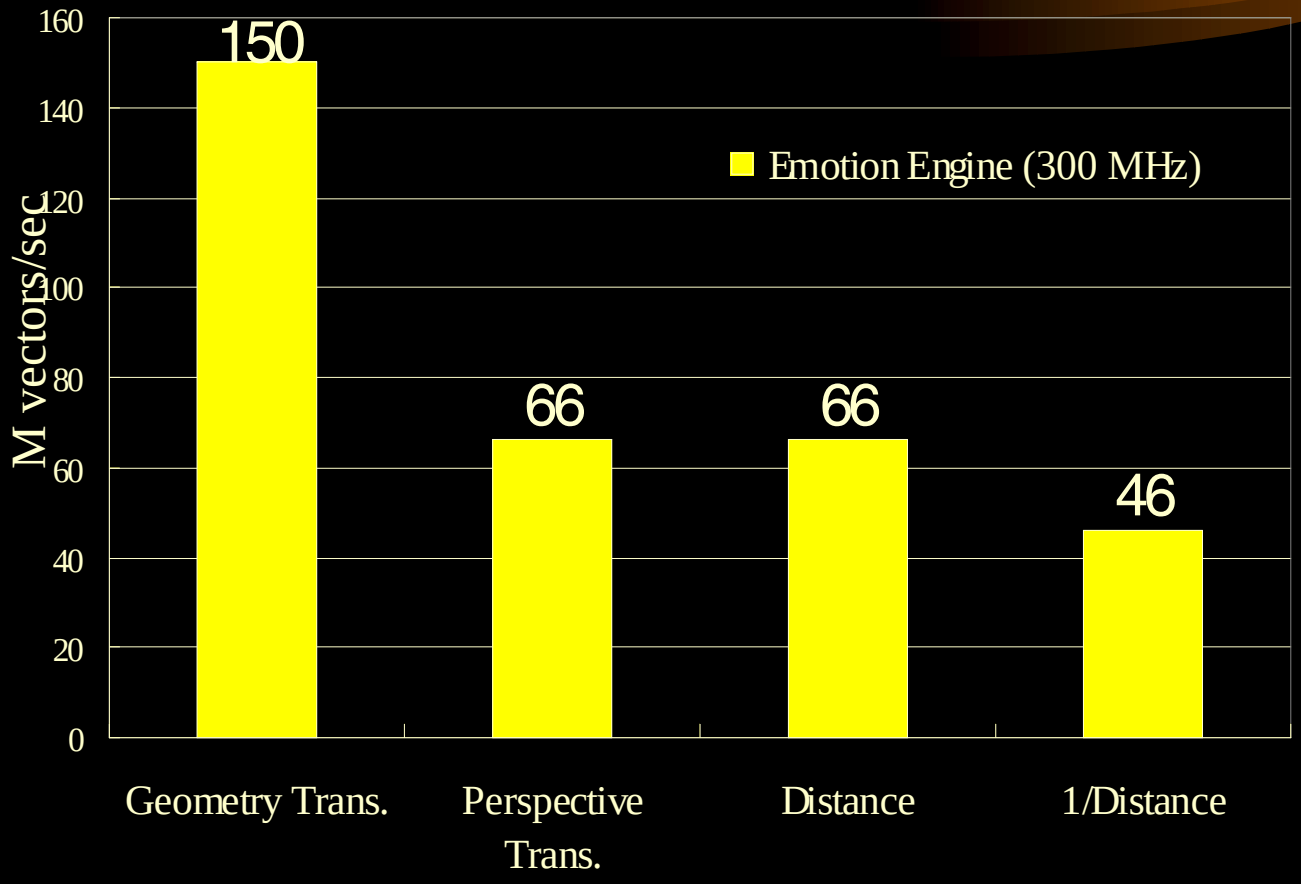
Example : Jelly

- Dynamic simulation

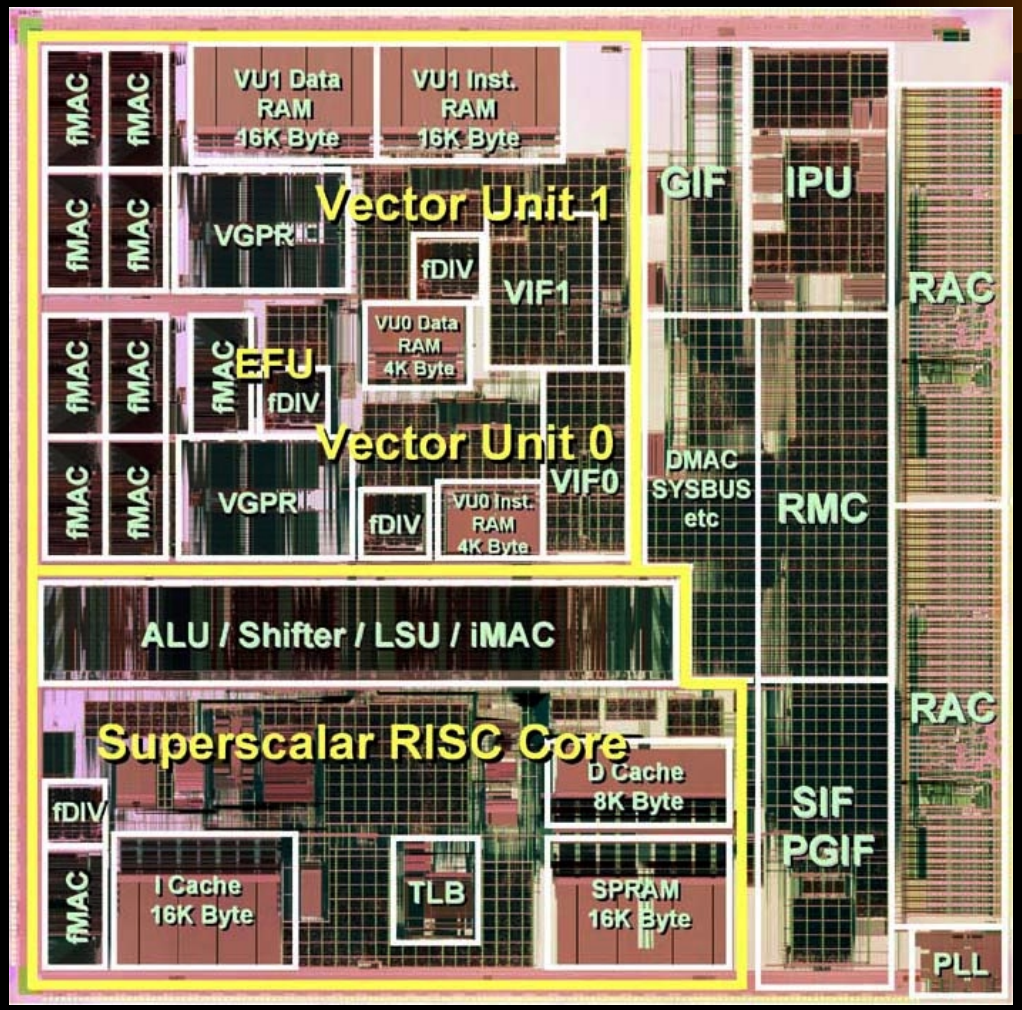


Spring model

Performance

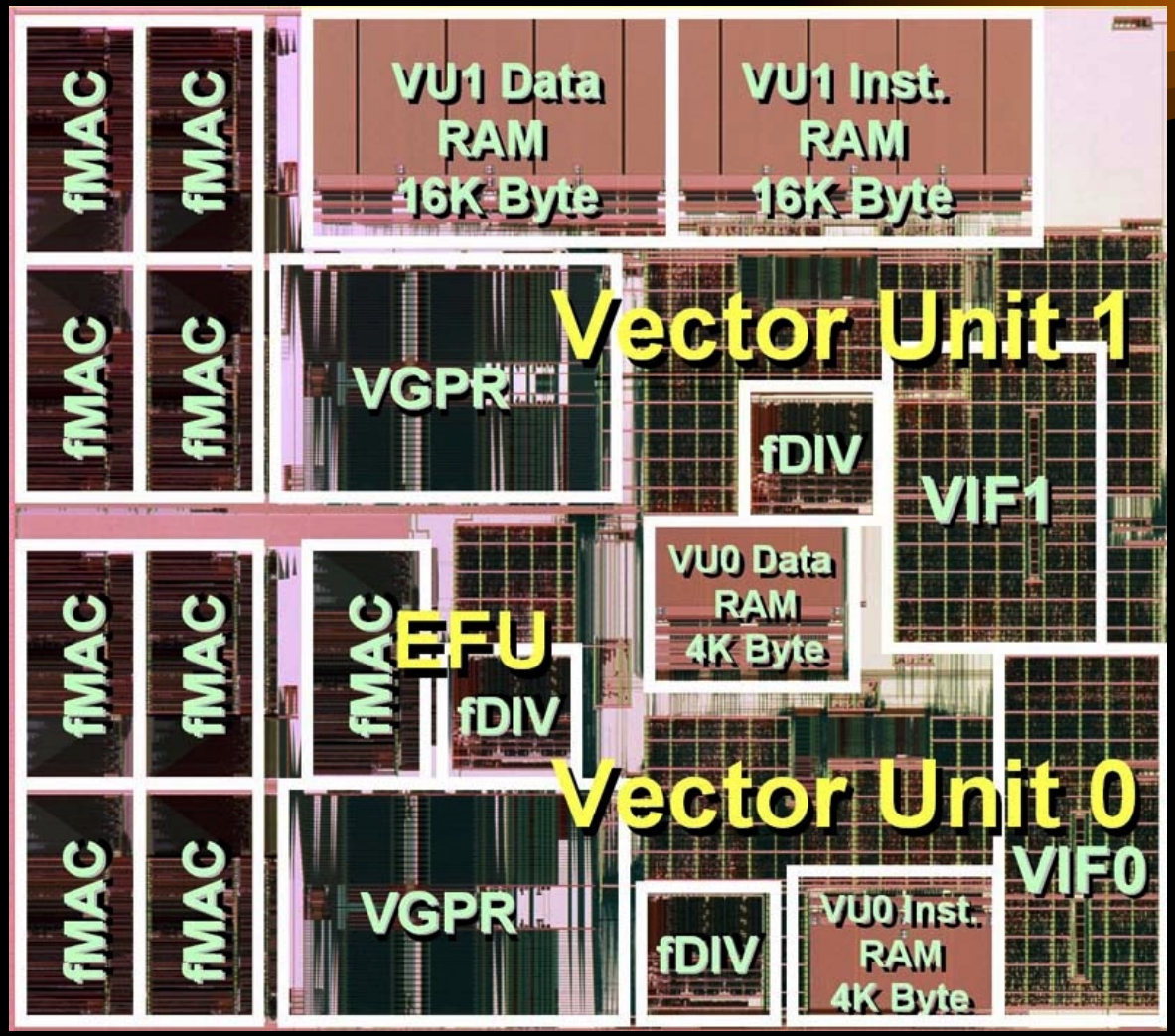


EE Micrograph



Die size : 15.02mm x 15.04mm
Frequency : 300MHz
Transistors : 13.5M
Power : 18Watts
Design Rule : 0.25um
Gate Length : 0.18um

VU Micrograph



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